VIEW POINT

# RISC-V: REDEFINING COMPUTING AND SEMICONDUCTORS

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## Introduction

The world of technology today is being disrupted by wave after wave of innovations, and various avatars of Generative AI, Large language models, Transformers, and AI-driven visual / video platforms such as Dall-E, Stable Diffusion, Bard etc are just the tip of the spear.

Semiconductor chips are integral to everything Digital and now powered by the Internet of Things (IoT), artificial intelligence, machine learning, 5G connectivity, and other emerging technologies, their use is increasing exponentially.

The growth of connected, smart devices bodes well for the semiconductor industry. Statistica.com estimates that the number of IoT connected devices will grow from 15+ billion in 2023 to ~ 29.42 billion by 2030. However, this poses a unique challenge – smart devices require custom processors (semiconductor chips) for their unique computing needs.

A majority of connected devices require specialized, modular processors that support custom instructions. Commercial-off-the-shelf (COTS) microprocessors often do not address specific requirements. This has compelled semiconductor chip designers to either develop chips themselves or make modifications to COTS products, akin to the familiar customization issue of ERP software programs.

## Brief history of processor architecture

Semiconductor chips are built on something very fundamental called the Instruction Set Architecture (ISA), which is the software that controls how the Central Processing Unit (CPU) or the computer functions. The ISA provides the pathway for the user to interact with the hardware. Currently, the market is dominated by 2 types of ISAs – the x86 and the ARM.

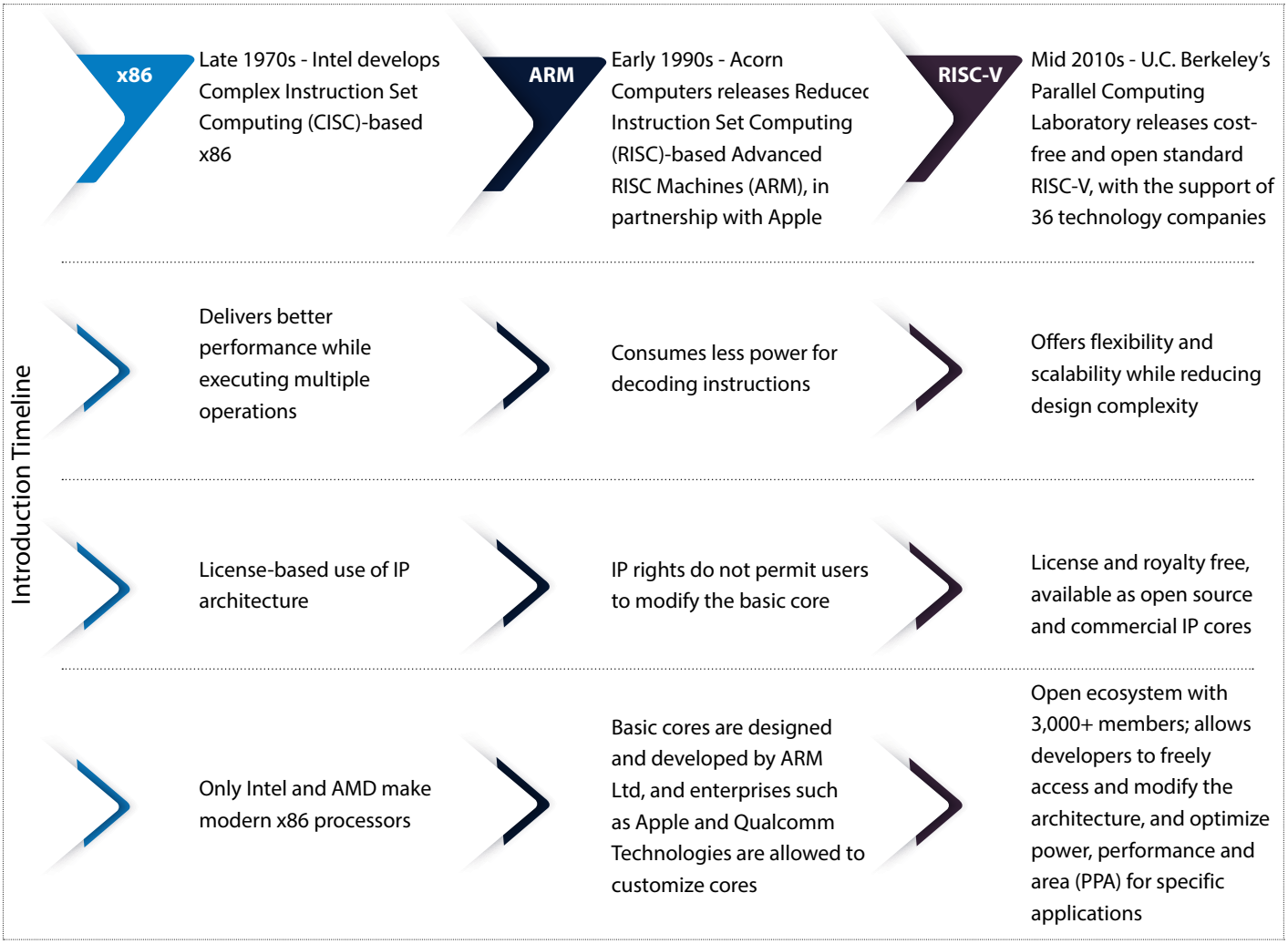
1. x86 had the first mover advantage. Released in 1970s, it is an IP architecture by AMD and Intel used primarily for desktops and laptops. Notably, Intel built an empire out of it and to this day, Intel still makes brand-new x86 CPUs using an ISA that is almost 50 years old
2. ARM - Competition to x86 was introduced in 1990s. In the ARM business model, the architecture was licensed to companies such as Apple and Qualcomm Technologies. ARM charges these companies licensing fees to use its technology to build their own chips (eg. Apple M1 and Qualcomm Snapdragon). It also earns royalty when these chips are produced and go into end devices. ARM processors are used in 99% of the smartphones manufactured worldwide.

While both these models have served their purpose very well, the need for an alternative ISA to keep pace with need for custom silicon has gained momentum over the years.

## RISC-V – An alternative

RISC-V (pronounced "risk-five") is an open standard instruction set architecture based on established reduced instruction set computer (RISC) principles. It is an open source and royalty-free ISA that was conceived in 2010 as a university project in UC Berkeley's Parallel Computing Laboratory. Eventually, 36 technology companies supported RISC-V and founded the RISC-V Foundation. Many implementations of RISC-V are available, both as open source cores and as commercial IP products. Companies are also allowed to make modifications to RISC-V cores.

The evolution of ISA and processor architecture features are summarized below:




## Why RISC-V is gaining momentum

The open source model of RISC-V ISA allows modifications to develop specialized chips for specific tasks. RISC-V supports the development of bespoke hardware to run software, and can be adopted in embedded applications and microcontrollers as well as high-performance computing systems and data centers. Further, the architecture fulfils the power requirements of space-constrained and battery-operated designs. The application options are infinite, and a majority of wearables, Industrial IoT devices and home appliances use chips designed through RISC-V. This is driving global demand for RISC-V technology. BCC Research predicts that the RISC-V technology market will grow at a CAGR of 33.1% to reach US$ 2.7 billion by 2027. By 2025 , 14% of CPUs are estimated to use RISC-V processors.

The business model of RISC-V challenges the status quo. Now, semiconductor designers have the liberty to select the ISA before partnering with a fabricator or building their own core. Further, new-generation systems providers can develop bespoke chips to support their unique service offerings without fees or license encumbrances.

The rise of RISC-V coincides with other industry milestones. Firstly, the deceleration of Moore's Law – total processing power is no longer increasing with each new fabrication node. Secondly, the widespread adoption of machine learning systems that require immense processing power. The only method to increase computational performance is via specialization. The open RISC-V ISA is modular and supports customized instructions, making it the ideal ISA to create a wide range of specialized processors and accelerators.

## The RISC-V ecosystem

Several nations and enterprises are investing in RISC-V technology to develop an efficient semiconductor ecosystem. The collaboration between industry stakeholders is accelerating open source processor development. Semiconductor leaders such as Qualcomm Technologies, NXP Semiconductors, Nordic Semiconductor, Robert Bosch, and Infineon Technologies are collaborating to fast-track development of RISC-V hardware. The joint venture is focusing on the automotive sector, and will expand to mobile and Internet of Things. Similarly, funding from Intel, Qualcomm, Western Digital, and SK hynix is empowering chip designers such as SiFive with resources for innovation in RISC-V-based high-performance systems. Western Digital is developing RISC-V-based controllers for hard drives and solid-state drives, which aims to provide significant performance and power consumption leverage vis-à-vis traditional x86 controllers. The European Commission is investing US$ 300 million via EuroHPC to develop RISC-V accelerators, tools and applications. The Digital India RISC-V (DIR-V) program fosters partnerships between startups, academia and multinational companies to design and develop RISC-V System on Chips (SoC) for servers, mobile devices, automobiles, IoT, and microcontrollers.

## Limitations of RISC-V architecture

While the open source architecture and license-free business model of RISC-V offer significant advantages, the risk of fragmentation is a key challenge.

The open instruction set for microcontrollers and microprocessors allows extensions to be added easily. It can lead to different versions, some of which may be incompatible with each other.

Verification of design is another challenge. Open source implementations must be vetted before SoC developers integrate it into chips. In the absence of a central team for designing and verifying RISC-V cores, emerging core suppliers need an independent verification solution to ensure that their designs are compatible with one another and comply with ISA specifications.

One of ARM's competitive strengths is its huge customer base of major technology providers. This has allowed ARM to build an ecosystem of companies that rely on its technology — an advantage that RISC-V does not have. Additionally, traditional players are skeptical about the preparedness of RISC-V for high-performance computing. They do not consider the technology to be mature enough to be a mainstream alternative to x86 or ARM.

## Future outlook

RISC-V holds immense potential in domains such as IoT devices, edge computing, artificial intelligence, and high-performance computing (HPC). Its modular design enables seamless integration with specialized accelerators for specific workloads, while ensuring efficiency and system performance. As chipmakers and fabless semiconductor companies recognize the benefits of RISC-V and embrace the open source philosophy to integrate computer chips into diverse objects, a broader spectrum of products that leverage this architecture will emerge.

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Venkat Srinivasan, is the Head of the Semiconductor, Electronics and Storage Business unit at Infosys. With deep domain expertise in the Semicon & Hitech industry, he is a trusted partner to C-level leadership. He brings with him deep expertise in technical & business functions, and has been relentless in his focus on driving solutions that address the 2 key imperatives of Time to Market and Cost of Revenue. He has helped clients solve complex problems pertaining to engineering, manufacturing, customer excellence and operational cost management, while helping them accelerate their vision to be global business leaders.

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